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# Evaluation of DVR Capability Enhancement-Zero Active Power Tracking Technique

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**ABSTRACT** This paper presents a utilization technique for enhancing the capabilities of dynamic voltage restorers (DVRs). This paper aims to enhance the abilities of DVRs to maintain acceptable voltages and last longer during compensation. Both the magnitude and phase displacement angle of the synthesized DVR voltage are precisely adjusted to achieve lower power utilization. The real and reactive powers are calculated in real time in the tracking loop to achieve better conditions. This technique results in less energy being taken out of the dc-link capacitor, resulting in smaller size requirements. The results from both the simulation and experimental tests illustrate that the proposed technique clearly achieved superior performance. The DVR's active action period was considerably longer, with nearly five times the energy left in the dc-link capacitor for further compensation compared with the traditional technique. This technical merit demonstrates that DVRs could cover a wider range of voltage sags; the practicality of this idea for better utilization is better than that of existing installed DVRs.

**INDEX TERMS** DVR capability, energy optimized, energy source, series compensator, voltage stability.

## I. INTRODUCTION

Recently in power systems, dynamic voltage restorers (DVRs) have been considered the most up-to-date series compensator for dynamically coping with a range of voltage variations. Their fast response is the main advantage of DVRs, which can fulfill most of requirements for sensitive loads. From a practical point of view, power systems with DVRs inside can elegantly provide a stable voltage for loads, for which better power quality can be guaranteed [1]–[6]. Additionally, lower power losses due to operation can be achieved compared to those with thyristor-based static compensators. Therefore, it can be stated that the DVR will remain a popular compensator for current power system improvement, where sensitive loads are increasingly installed. To gain more from DVRs, proper ratings must be considered in order to cover all of the voltage changes. Additionally, the control technique needs to be considered, as different compensation concepts will result in different performances [3], [7]–[11].

According to some recent applications, the sizing of standard DVRs depends on two main factors – load and nature of voltage sags, both magnitude and existing period [12]–[15]. Whenever the system voltage is decreased, DVRs will respond by supplying some power to the load side. Load ratings are then prioritized by specifying the selections of DVRs. The severity of voltage sag is also an important concern. A range of voltage drops between 0.1 and 0.9 per-unit will certainly result in different amounts of compensating power needed from the DVR; higher severities require more power. Lastly, the length of the voltage sag must be considered. Smaller DVRs may not be able to cover the entire length of sags according to stored energy in the DC-link capacitor. This means that energy utilization behavior will affect a DVR's performance. Smarter techniques can make the most of the limited energy.

Including a converter inside a DVR as a controllable component allows the DC-link capacitor to play a major role. In power system applications, insufficient energy stored in this capacitor means that the DVR cannot address demands during the compensation. The compensation may not fulfill all of the requirements to maintain the voltage corrections. Moreover, for some cases, the stored energy may or may not be sufficient to cover and last for the entire sag period, which is the main reason why the DC-link capacitor is so important for this kind of application. Selection of a large or small capacitor, however, requires economic

consideration [16]–[19]. A compromise between cost and ability to cover voltage sags has been considered so far.

Insight into the operation of DVRs is therefore needed, not only the abovementioned energy the DC-link capacitor provides but also the energy loss due to the switching operation of the voltage source converter [20] used in the compensation. Thus, any way to keep it lower or even to get rid of it will possibly give the DVR more capability. This would also reduce the cost of DVRs with a smaller capacitor inside. In this paper, one important factor is to make it possible to adjust tracking for the best DVR output in order to achieve pure reactive power compensation. Then, ideally, little or no real power will be utilized for the compensation process, except the loss that is unavoidable. The explicit outcome is less energy taken out of the DC-link capacitor. Longer lasting active compensation can reasonably be expected.

In spite of having some satisfactory compensation techniques, requiring better performance with the ability to cover more severe voltage sags appears to be a major issue among modern utilities. Enhancement for longer lasting compensation is required. This paper then responds with a technique for the control of DVRs with zero active power tracking compensation, which will be discussed in-depth. Real-time non-linear control is applied to provide the best compensation tracking. Both the magnitude and displacement of the voltage are controlled by approaching two possible targets, as described in the proposed technique section. The advantages gained from this zero-active power compensation will make the DVR a potentially beneficial device. This technique will contribute benefits to existing DVR-based compensation. Contents covered in this paper focus on the compensation concept and its corresponding control system. Clear results from both simulation and experiment are illustrated comparatively with a traditional DVR.

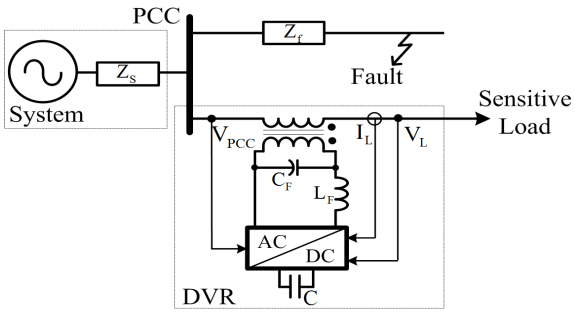


**FIGURE 1.** Single-line diagram of a power system with the DVR connected at PCC.

## II. STRUCTURE AND OPERATION OF A DVR

A DVR is a dynamic power compensator that has been practically applied in many modern power systems in order to stabilize the voltage provided for loads at specific locations [18], [19]. It is series-connected between the point of common coupling (PCC) and loads (mostly sensitive ones), as illustrated with a simple system schematically in Fig. 1, where a series connected insertion transformer functions as a coupling component. Therefore, to compensate for the better voltage, it must modulate the output of this transformer. By using a control technique as the key to provide for all possibilities that the bi-directional DC-to-AC power converter can produce, the compensating voltage will be the correct one added up to the sag when responding to the system voltage variation. For the converter, only a capacitor is used as the DC-link at its DC-side supplying energy out to the system during compensation. An LC-filter is used to mitigate any unwanted content due to switching effects before passing the synthesized voltage to the coupling transformer, finally acting as a corresponding compensator.

When activated, the DVR will monitor if the load current ($I_L$), load voltage ($V_L$), and system voltage at the PCC ($V_{PCC}$) are all in an acceptable range. If a disturbance occurs, which is mostly caused by the nearby faults, $V_{PCC}$ will be suddenly decreased, a consequence due to voltage drop at the system and line impedance ($Z_S$ and $Z_F$). Often, not only is the magnitude of the voltage changed but also its associating phase displacement angle is reasonably shifted. In technical terms, the voltage drop and phase shift are generally called ''voltage-sag'' and ''phase-jump'', respectively. Both of them appear to be problems that result in concerns of poor power quality. Therefore, without compensation or any correction, the voltage to load is equal to the sag voltage (poor quality is directly passed to loads). However, if the DVR detects this, it will try maintaining a condition that keeps the voltage at least in the acceptable range or even the rating, depending on its capability.

In principle, to correct the voltage problem, as desired, some of the real and reactive power will be circulated between the DVR and the system in order to provide the best output for loads. In summary, generally two different DVR-based compensation techniques are applied, as described in detail in the following sections of this paper.

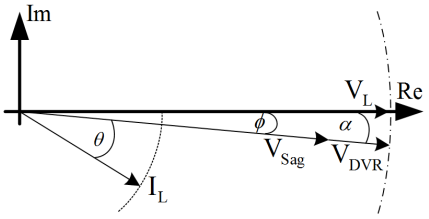


**FIGURE 2.** In-phase compensation.

### A. IN-PHASE COMPENSATION

The in-phase compensation means that a representing phasor of the compensating voltage generated by the DVR is aligned with the sag voltage phasor, as illustrated in Fig. 2. It can be seen that the DVR voltage, VDVR, is generated by precisely adding up to be in-phase with the sag voltage, $V_{Sag}$. As a consequence, this compensation results in the magnitude of load voltage levelling up to its normal rating (the pre-sag voltage), as is predefined. With these phasors, calculations

for the power utilization from the DVR during compensation are given in (1) and (2).

Both the real and reactive power ($P_{DVR}$ and $Q_{DVR}$) utilized are associated with the compensation required in order to steadily provide a compensating voltage during the disturbance. According to (1) and (2), the displacement angle between the compensating voltage and load current phasors is one of the key indicators of how much power will be utilized in providing a better voltage for all the particular loads. The compensation period and amount of energy consumed can also be determined directly from the voltage $V_{DVR}$ magnitude. As seen in Fig. 2, when the magnitude of load voltage is increased, the load current is also increased up to its normal desired value. The displacement angle ($\theta$), which is tied to the voltage, is then slightly shifted. It can be seen that the magnitude of the DVR voltage is the key parameter dominating how much power is transferred from the DVR to the AC-side.

Therefore, it can be said that, as described by the diagram illustrated in Fig. 2, although the sag voltage can be mitigated by the DVR and the resulting load voltage is back to an acceptable value, the active compensation may not last for a long duration, as the stored energy in the DC-link will be utilized quickly in this technique. The DVR may deal only with some short period voltage sags.

Furthermore, according to the in-phase compensation phasor illustrated in Fig. 1, (1) and (2) also indicate that the load power factor (the multiplier $\cos\theta$) will have a larger effect on the compensation performance. High power factor loads lead to more energy being used to maintain a constant voltage – a lower $\theta$ yields quite a high $P_{DVR}$ being injected into the system. Clearly, with this mathematical evidence, it is also evident that the DVR's performance is unavoidably deteriorated by the load characteristics.

$$P_{DVR} = |V_{DVR}|\, I_L \cos(\theta) \tag{1}$$

$$Q_{DVR} = |V_{DVR}|\, I_L \sin(\theta) \tag{2}$$

### B. PRE-SAG COMPENSATION

To overcome the two compensation issues mentioned previously – phase jump and load dependence, another technique called pre-sag compensation has therefore been introduced. This technique was proposed with the ability to adjust both the magnitude and phase of the compensating voltage generated by the DVR in order to enhance the overall performance of the traditional in-phase technique. For this compensation, whenever a noticeable change of the system voltage is detected, the control system will activate the operation of the power converter in order to generate a more flexible voltage $V_{DVR}$, as shown in Fig. 3, in which the corresponding phasor of the compensation indicates that the compensating angle is shifted by $\alpha$, aiming to increase and align the load voltage with the "pre-sag" or its normal rated value.

Adding the DVR voltage finally results in the load voltage $V_L$ phasor being stretched relative to its pre-sag alignment condition, as shown in the diagram. Clearly, the magnitude then returns to the load rating (dotted curve of the circle), and the phase-jump is eventually corrected, with its phasor placed exactly at the zero degree reference being the same as its pre-sag condition. In more detail, this compensation technique precisely operates the DVR with equations (3) – (6).

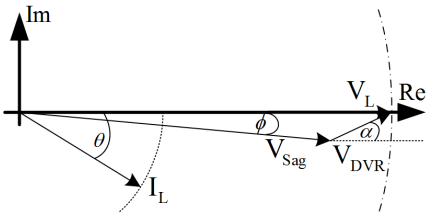


**FIGURE 3.** Pre-sag compensation.

Real and reactive powers are required for supporting a proper compensation, as shown in the diagram of Fig. 3. The $V_{DVR}$ phasor is the correct one for the compensation. During this process, the amount of real power from the DVR, $P_{DVR}$, in (5) implies that the energy stored in the DC-link capacitor is used depending on the load current instance and its displacement angle, which is with respect to the DVR voltage phasor displacement.

By this technique, the resulting displacement angle between the DVR voltage and load current phasor is increased considerably by the summed angle $\alpha$. Equation (5) then obviously yields a lower $P_{DVR}$ being taken out of the DC-link capacitor, indicating that less DC-link energy is consumed than in the in-phase compensation of (1). This mathematical confirmation demonstrates the possibility of longer lasting compensation from this pre-sag compensation.

$$|V_{DVR}| = \sqrt{V_L^2 - 2V_L V_{Sag}\cos(\phi) + V_{Sag}^2} \tag{3}$$

$$\alpha = -\tan^{-1}\left(\frac{V_{Sag}\sin(\phi)}{V_L - V_{Sag}\cos(\phi)}\right) \tag{4}$$

$$P_{DVR} = |V_{DVR}|\, I_L \cos(\alpha + \theta) \tag{5}$$

$$Q_{DVR} = |V_{DVR}|\, I_L \sin(\alpha + \theta) \tag{6}$$

Then, it is reasonable to expect that according to the principle mentioned above, adding up a stretchable phasor in a pattern of modifiable phase shifting to the sag voltage will be able to achieve a lower or even zero real power compensation process, which aims to increase the DVR capability in order to address a wider range of voltage sags. Details of this proposed technique are described clearly in the following sections.

## III. THE PROPOSED COMPENSATION TECHNIQUE

The goal of zero active power tracking for enhancing DVR-based compensation is to make the most of the utilizable energy ($\Delta W_{DC}$) that is stored in the DC-link capacitor. This limited energy can be calculated as in (7); due to technical limitations, not all the stored energy can be utilized. The minimum DC-side voltage ($V_{DCmin}$) must be at a level that can still provide the converter with proper operation. Anything lower than this level will result in the converter

not producing the demanded AC voltage. In practice, this value can be defined as in (8). In addition, by the principle of DC-to-AC power conversion, the maximum DC voltage ($V_{DCmax}$) at the DC-link should increase proportionally to the AC-side voltage ($V_{DVR}$) required for every instant active compensating actions.

According to these two equations, the compensation period ($T_C$) can be given as in (9), which shows that more utilizable energy yields longer active compensation for the DVR to address sags. Obviously, less real power utilized by the DC-link capacitor means that the DVR can also last for a considerable period and overcome more of the voltage sag.

$$\Delta W_{DC} = \frac{1}{2}C\left(V_{DCmax}^2 - V_{DCmin}^2\right) \tag{7}$$

$$V_{DCmin} \geq \sqrt{2}V_{DVR} \tag{8}$$

$$T_C = \frac{\Delta W_{DC}}{P_{DVR}} \tag{9}$$

Therefore, in order to gain more from the DVR, the idea proposed here is to achieve a condition where the compensation process requires the least real power from the DC-link capacitor.

### A. ZERO ACTIVE POWER TRACKING

As mentioned earlier, varying both the magnitude and phase of the DVR voltage plays a major role in reaching better compensation for the sag voltage. This voltage is involved in the calculation of energy stored in the DC-link capacitor that would be utilized each moment, as indicated in (1)-(6). Considering these equations, to achieve the best performance, the displacement of the corresponding DVR's voltage and load current complex phasors must be maintained at an angle of approximately 90 degrees, as illustrated in Fig. 4, ideally following calculations using (1) and (5) for zeroing the utilized energy on its own.

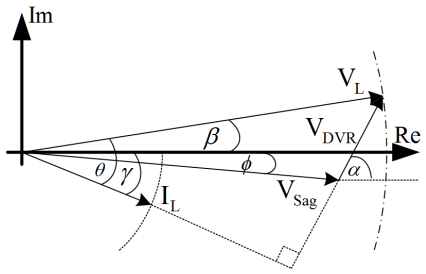


**FIGURE 4.** Zero active power tracking compensation.

The illustration in Fig. 4 also shows that the DVR voltage phasor is a stretchable one, as required, representing the compensation voltage added to the sag voltage. Its magnitude is adjusted related to the calculation of (10), and its displacement angle $\alpha$ is set according to (11). An angular displacement $\gamma$ indicates the load characteristic, which can be determined directly using (12), relating to the load real power. Similar to the angle $\theta$ displacement, it is also tied to the resulting voltage. Therefore, adjusting the DVR voltage will result in both $\theta$ and $\gamma$ being changed. By this technique, the resulting load voltage phasor may or may not be returned to the pre-sag level; some $\beta$ degrees displacement must be observed.

The tracking process starts with the control of the converter output to provide the corresponding voltage, which must be varied to meet the targets. The magnitude and phase are increased progressively until reaching a value that results in a relatively acceptable power. Two possible targets are set as the preferred tracking boundaries. In case 1, the ideal zero active power ($P_{DVR} = 0$) is achieved, while the load is still supported by some of the system reactive power. In this case, the load current lags behind the grid voltage (the sag voltage, $V_{Sag}$). In case 2, the minimum active power is achieved (as it cannot achieve zero active power), whenever all of the load reactive power is completely supported by the DVR and no longer supported by the system. At that point the load current appears to advance in leading the voltage sag, which indicates that the DVR not only supplies to the load side but also begins supplying reactive power back to the grid side. The increase in the phase angle $\alpha$ should be stopped immediately. If not, high power loss will degrade the DVR performance.

Reconsidering the phasors of voltage and current shown in Fig. 4, it can be concluded that the normal and light voltage sags could possibly result in case (1) - the compensation eventually results in the zero reactive power condition. If the voltage sag is deep in a severe example, the compensation could result in the minimum power case 2.

The effectiveness of this compensation process is directly reliant on a proper control system that assists the entire tracking process in order to achieve the mathematical targets detailed in the following (10)-(15).

$$|V_{DVR}| = \sqrt{V_L^2 - 2V_L V_{Sag}\cos(-\theta+\gamma+\phi) + V_{Sag}^2} \tag{10}$$

$$\alpha = \tan^{-1}\left(\frac{V_L\sin(-\theta+\gamma) - V_{Sag}\sin(\phi)}{V_L\cos(-\theta+\gamma) - V_{Sag}\cos(\phi)}\right) \tag{11}$$

$$\gamma = \phi - \cos^{-1}\left(\frac{P_{Load}}{V_{Sag}I_L}\right) \tag{12}$$

$$P_{DVR} = V_{DVR}I_L\cos(\alpha-\gamma) = 0 \tag{13}$$

$$Q_{DVR} = V_{DVR}I_L\sin(\alpha-\gamma) \tag{14}$$

$$Q_S = V_{Sag}I_L\sin(\gamma-\phi) \tag{15}$$

### B. CONTROL SYSTEM

Assisting the converter in order to generate a suitable voltage for the compensation, where less real power is output from the DVR, is the main objective of this control tracking system. The correct compensating voltage must be met by the mentioned targets. In searching for the desired condition, a fuzzy logic based controller (FLC) is employed to provide a proper phase angle for the required voltage, dealing with non-linearity due to the incremental phase displacement.

Referring to the phasor diagram illustrated in Fig. 4, when the angle $\beta$ is increased with respect to the zero degree

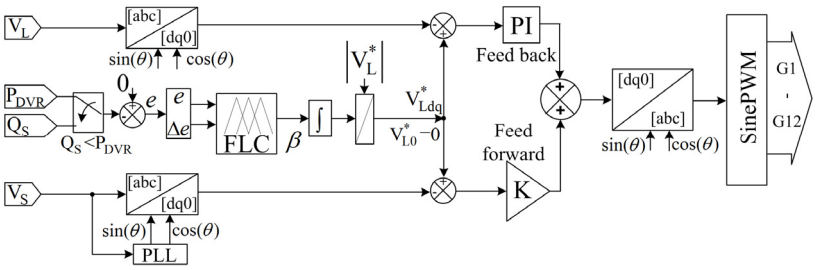


**FIGURE 5.** The proposed control system.

reference, the corresponding power also increases but not proportionally. In accordance with the principle described previously, a precise increment of the angle $\beta$ phase shifting of the demand voltage will be obtained from the FLC, as shown in Fig. 5, where the relevant power error was then processed to provide for the phase shifting.

A standard PI feedback loop, with its corresponding feed-forward, is used to provide the corresponding controlled signals for generating the required voltage. For this project, the Ziegler Nichols tuning heuristic method [21] is applied for the standard PI controller loop, while the gain K is set depending on the DC-link capacitor normal voltage rating. The transformability of voltage signals between stationary and rotating frames of reference, abc-to-dq0, is also employed to monitor and decompose the in-phase and quadrature voltage or the real and reactive components ($V_{Ld}$ and $V_{Lq}$). $P_{DVR}$ and $Q_S$ are further evaluated.

The controlled DVR voltage signals are then passed to the converter switching control, which is used to generate the required voltage that the compensation requires. Therefore, gating signals $G_1$-$G_{12}$ in Fig. 5 are passed to switching devicesin the converter (typically the IGBTs) for the sine wave PWM strategy for this project. The FLC will continue to provide the incremental angle $\beta$ unless either the ideal zero active power from the DVR is met or zero reactive power from the system is approached. Finally, whichever case is approached first, the condition will be maintained for the rest of the compensation period until change in voltage sag is detected; at which time, the tracking process will be repeated again.

## IV. SIMULATION

The corresponding system for verification of the proposed compensation technique was modelled in MatLab/Simulink/PowerSys for comparison with the traditional technique, as shown in the schematically simplified diagram in Fig. 6. The main components in this system are full-bridge power converters with LC filters and DC-link capacitor (C) included, three insertion transformers used as coupling devices series-connected between a three-phase power supply and a lagging power factor load, and the control that monitors the system voltage ($V_{PCC}$), load voltage ($V_L$) and current ($I_L$), as mentioned previously.

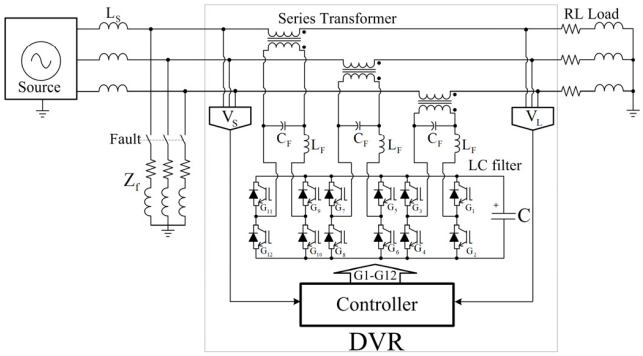


**FIGURE 6.** Circuit diagram model for simulation using MatLab/Simulink.

**TABLE 1.** Parameter ratings for simulations and experiments.

| Quantity | Value |
|---|---|
| $V_S$ | 380V |
| Load | 2.33kVA, 0.45 lagging |
| DC- link Capacitor | 3.3 mF |
| LC Filter | 1mH, 20uF |
| $Z_f$ | 0.43 Ω 1mH |

Output signals from the control ($G_1$-$G_{12}$) were used for further gating of all the IGBTs in order to have the synthesized compensation voltage at the insertion transformer terminals, according to the technique employed.

In comparison to this simulation, all the model's parameters were established relative to the overall test rig availability for the experimental tests and were scaled to available laboratory ratings. As shown in Table 1, a three-phase programmable supply of up to 380 V AC was used as the system source voltage ($V_S$). The simulations were then conducted comparatively, as described in subsections A and B.

### A. THE TRADITIONAL IN-PHASE COMPENSATION

For comparison, the traditional in-phase compensation was conducted first, highlighted by the remaining energy in the DC-link capacitor and duration of the proper supporting voltage that was being generated by the DVR during the compensation. For clarity, the highlights occurred with voltage sag. For example, the drop in $V_S$ between t = 0.4 s and 0.9 s, which was seen as $V_{Sd}$ (direct-axis voltage), is illustrated in

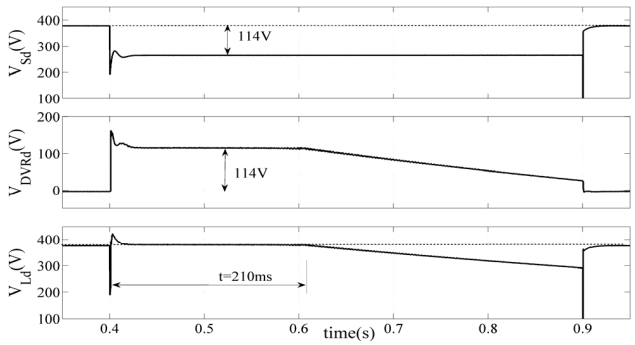


**FIGURE 7.** D-axis voltages at the system ($V_{Sd}$), DVR ($V_{DVRd}$), and load ($V_{Ld}$). during in-phase compensation (simulation).

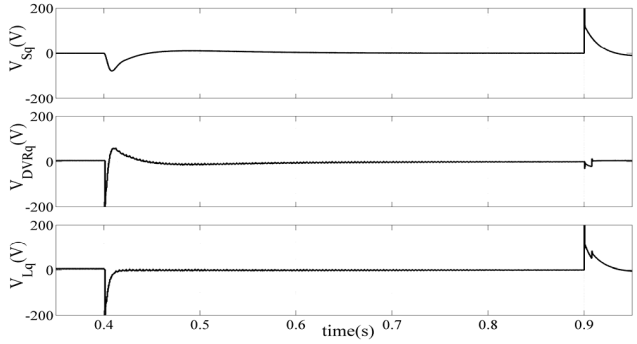


**FIGURE 8.** Q-axis voltages at the system ($V_{Sq}$), DVR ($V_{DVRq}$), and load ($V_{Lq}$) during in-phase compensation (simulation).

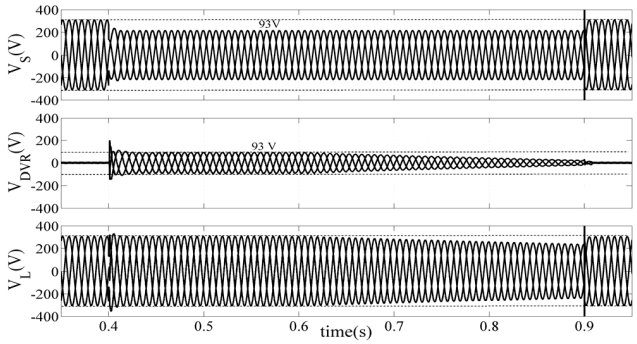


**FIGURE 9.** The overall three-phase voltage signals during in-phase compensation (simulation).

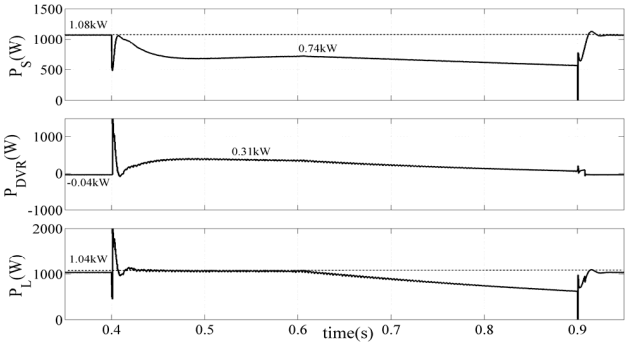


**FIGURE 10.** Real power at source ($P_S$), the DVR ($P_{DVR}$) and load ($P_L$) during in-phase compensation (simulation).

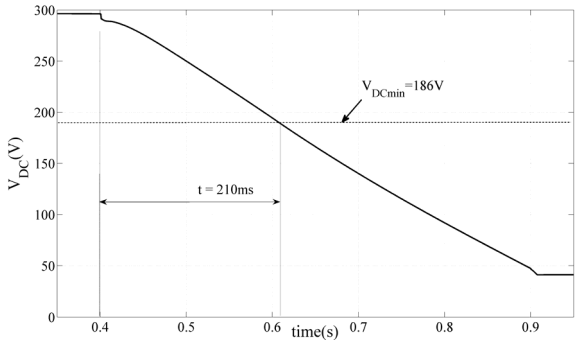


**FIGURE 11.** The DVR DC-side voltage ($V_{DC}$) during in-phase compensation (simulation).

Fig. 7. Then, at t = 0.4 s, the load voltage was at 114 V, which was lower than the rated $V_L^* = 380$ V.

In response to this, the DVR injected an exact compensating voltage ($V_{DVR}$) immediately after the DVR detected the mentioned sharp drop in the $V_{Sd}$. Afterwards, as a result, the load voltage was then increased to the desired value. As can be seen, this was the in-phase technique compensation. All the quadrature components of the relevant voltages were zero, as shown in Fig. 8. Therefore, the direct-axis voltage directly represents the magnitude of the load voltage, resulting in the corresponding three-phase voltage increase shown in Fig. 9. The magnitude was the same as the trend in direct-axis voltage captured, as shown in Fig. 7.

Related to this process, the overall real power flows were captured, as shown in Fig. 10, in order to consider how long the DVR could cover for the compensation. Real power flows were agreeable to the voltages plotted in both Figs. 7 and 8. It can be clearly seen that real power $P_{DVR}$ was associated with the energy output of the DVR provided for the compensation.

When the sag occurred, the load was able to consume power at its own demand only in the first 245 ms of the entire voltage sag.

When the compensation started, stored energy in the DC-link capacitor was used to generate AC voltage at the corresponding converter. Then, the DC-side voltage reduced proportionally to the utilized energy, as shown in Fig. 11. Nonetheless, this satisfactory compensation continued for approximately 245 ms until approximately t = 0.64 s, when the DC-side voltage decreased to the minimum value of approximately 186 V. It can be seen that if it is lower than this value, the DVR could no longer provide a proper compensating voltage in order to maintain the desired compensation.

Consequently, as seen in Fig. 7, from time t = 0.64 s to t = 0.9 s, the bottom waveform shows that the load was being fed with under-voltage. It is clear that the compensation could not last for the whole voltage sag period. According to this evidence, it is implied that a portion of the voltage sag may not be covered by in-phase compensation techniques.

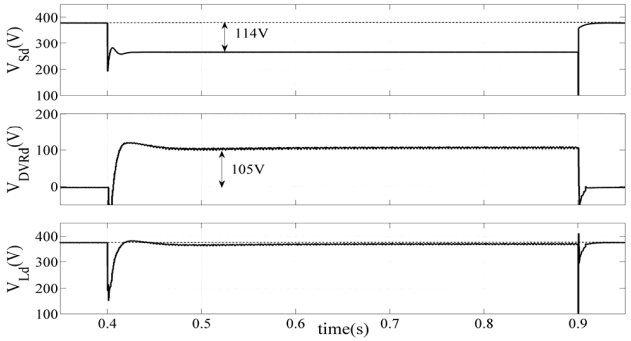


**FIGURE 12.** D-axis voltages at the system($V_{Sd}$), DVR ($V_{DVRd}$), and load ($V_{Ld}$) during zero-real power tracking compensation (simulation).

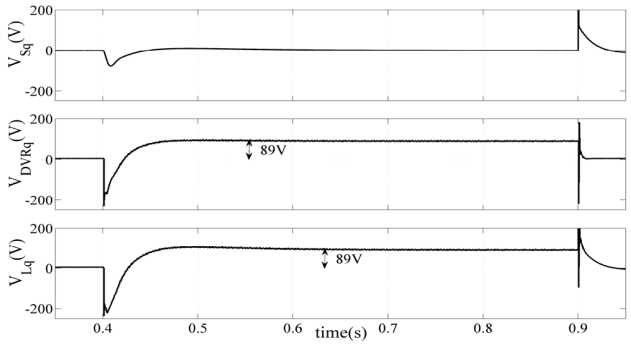


**FIGURE 13.** Q-axis voltages at the system ($V_{Sq}$), DVR ($V_{DVRq}$), and load ($V_{Lq}$) during zero-real power tracking compensation (simulation).

### B. THE PROPOSED COMPENSATION

In order to extend the compensation as described in the previous sections, the proposed technique of zero-real power tracking was implemented with the same system mentioned in subsection A instead of the in-phase technique. The same simulation procedures were conducted, and the results were captured, as shown in Figs. 12-16. It is clear that different results were seen.

The middle trace in Fig. 12 shows that by this technique, the DVR can certainly cover the entire voltage sag period, from the beginning at the time t = 0.4 s to the end at time t = 0.9 s. The associated quadrature voltages of both the DVR output and load point illustrated in Fig. 13 were increased and given the relevant voltages levelled back to the desired value, as expected. It can be seen that the resulting three phase load voltage (the bottom waveform of Fig. 14) remained constant during the demand and after the sag period. The bottom trace of Fig. 15 shows that the load was therefore fed with its rating power even during the deep sag period, which was a promising result.

According to this technique, much lower real power was drawn from the DC-link capacitor, which resulted in relatively less energy being output for the instant compensation. Therefore, the decrease in DC-side voltage at the DC-link was not considerable, as seen in Fig. 16, compared with in-phase compensation illustrated in Fig. 11. Only a 50 V drop is seen, compared to 250 V for the in-phase technique. These numbers

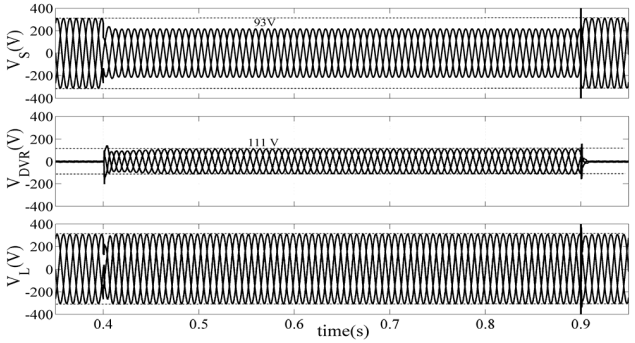


**FIGURE 14.** The overall three-phase voltage signals during zero-real power tracking compensation (simulation).

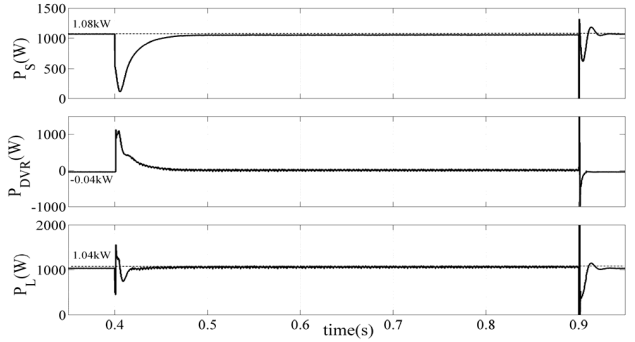


**FIGURE 15.** Real power at source ($P_S$), the DVR ($P_{DVR}$) and load ($P_L$) zero-real power tracking compensation (simulation).

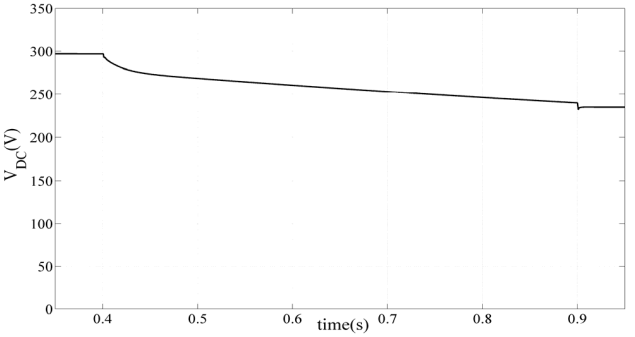


**FIGURE 16.** The DVR DC-side voltage ($V_{DC}$) during zero-real power tracking compensation (simulation).

imply that a considerable amount of energy remained for possible further compensation.

## V. EXPERIMENTAL TESTS

As mentioned earlier, validation of the proposed idea would be carried out comparatively. The test circuit diagram is shown in Fig. 17 – a programmable voltage sag generator was used to provide the input voltage sag for the experiments, a system inductance ($L_s$) of 1.0 mH connected between the source and the PCC where a series transformer was used to link the DVR to the system and 2.33 kVA 0.45 lagging R-L load. IGBTs #IRG4PH40UD were circuited as single-phase full-bridge voltage source inverter (VSI) with 3.3 mF DC-link capacitor. LC filters of 1.0 mH and 20 uF were

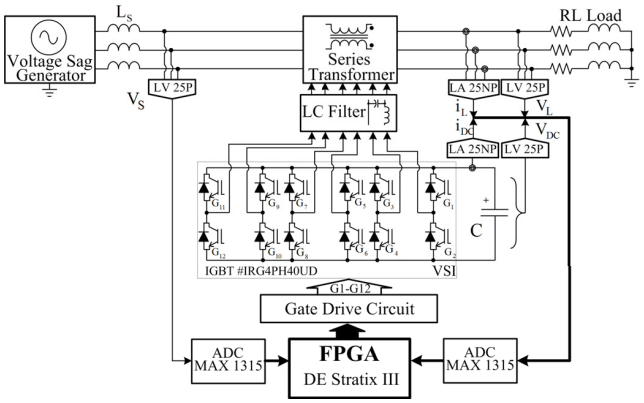


**FIGURE 17.** Circuit diagram of the overall test rig.

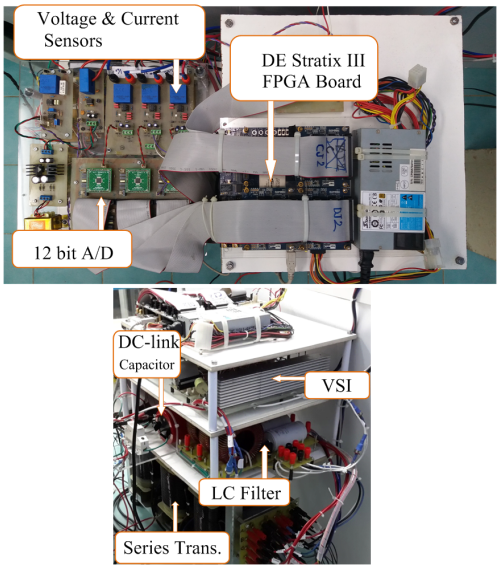


**FIGURE 18.** The overall test rig.

added to the output of the inverter. Current and voltage sensors (LEM LA25NP and LV25P) were used for acquiring the required voltage and current signals for the control loop through ADC Max1315 (12-bit A/D). FPGA DE Stratix III [22] was used as the main control component to perform both the loop controller and Fuzzy logic based tracking for the best injection of real power, as described in the simulation.

The overall test rig described above referring to the circuit diagram depicted in Fig. 17 is shown in Fig. 18. The implementation was carried out comparatively, described in the two following subsections.

### A. THE IN-PHASE COMPENSATION TEST

The traditional in-phase compensation technique was first carried out with the same procedure as described for the simulations. For this, the experimental test was highlighted with a sudden drop in the system voltage between t = 0.4 s and t = 0.9 s. The system direct-axis voltages at the PCC and the DVR and the load voltages were measured and re-plotted

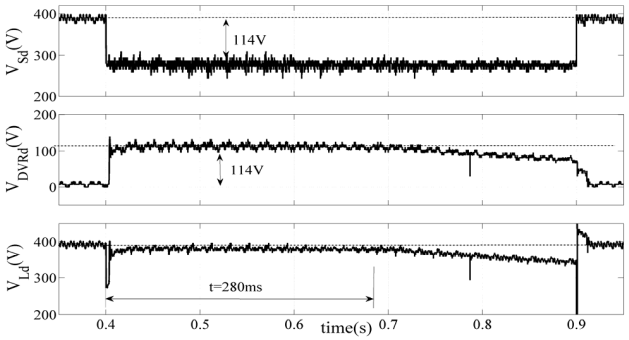


**FIGURE 19.** D-axis voltages at the system ($V_{Sd}$), DVR ($V_{DVRd}$), and load ($V_{Ld}$) during in-phase compensation.

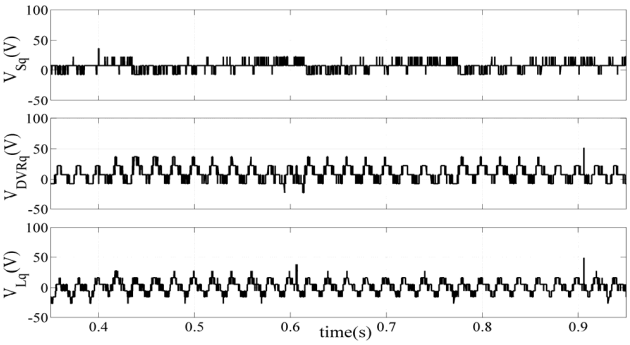


**FIGURE 20.** Experimental result of voltage base on q-axis at source, DVR and load– In Phase Compensation.

as the waveforms shown in Fig. 19. Similar to the simulation results, as expected, the voltage at load varied relative to the system voltage during this highlighted period.

Waveforms plotted in Fig. 19 show that the DVR did not complete the compensation; it lasted for only the first 280 ms, not for the whole period as desired. It is understandable that according to this technique, the stored energy was output directly from the DC-link capacitor in the form of real power flow (no reactive power was involved, as seen in Fig. 20, in which the quadrature voltage was not generated from the DVR). Then, when reaching its limitation, both the compensations and load voltages (the middle and the bottom traces shown in Fig. 19) decreased gradually from the time t = 0.7 s onwards. As a result, the overall three phase voltage did not remain constant at the desired level, as shown in Fig. 21. The highlighted 280 ms period was marked to indicate the period the proper compensation lasted.

For this case, as mentioned in the simulation sections, the magnitudes of the three phase voltages depended mostly on the direct axis voltage, which is plotted in Fig. 19. It is evident that this compensation was limited to the inside energy stored in the DC-link capacitor, as shown in Fig. 22, where all the real power the DVR was trying to inject into the system during the sag period seemed to fail to continue after 280 ms. It could not provide the desired amount.

Related to the reduction of the stored energy in the DC-link capacitor, the DC-side voltage dropped noticeably, as shown in Fig. 23, the drop from the initial to the minimum

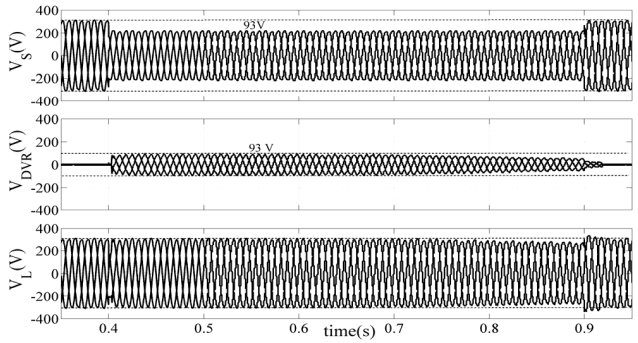


**FIGURE 21.** The overall three-phase voltage signals during in-phase compensation.

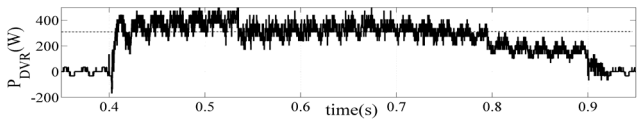


**FIGURE 22.** Real power from the DVR ($P_{DVR}$) during in-phase compensation.

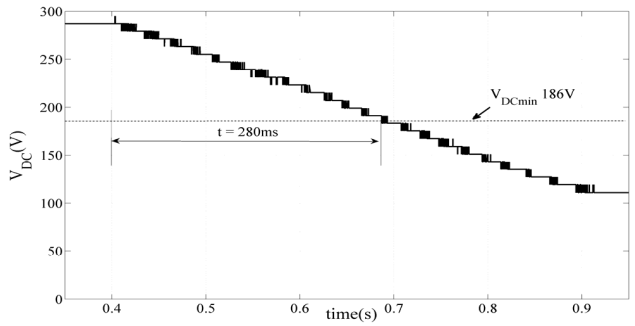


**FIGURE 23.** The DVR DC-side voltage ($V_{DC}$) during in-phase compensation.

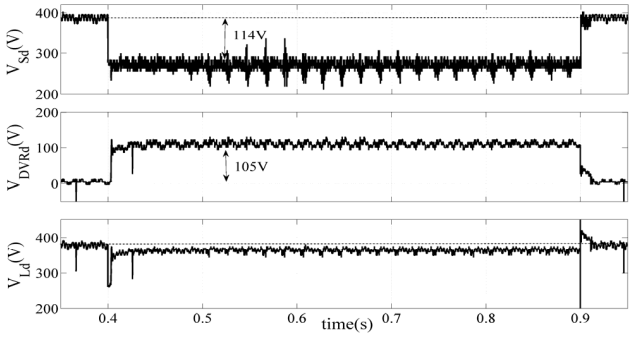


**FIGURE 24.** D-axis voltages at the system ($V_{Sd}$), DVR ($V_{DVRd}$), and load ($V_{Ld}$) during zero-real power tracking compensation.

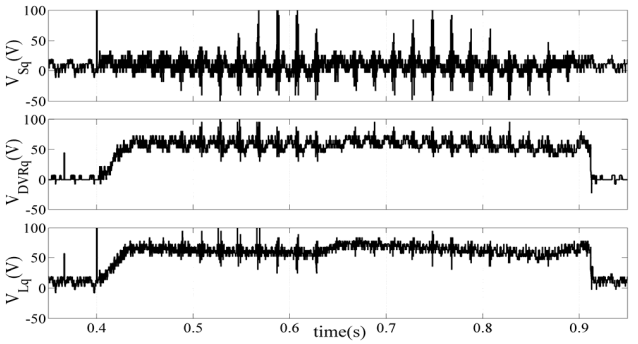


**FIGURE 25.** Q-axis voltages at the system ($V_{Sq}$), DVR ($V_{DVRq}$), and load ($V_{Lq}$) during zero-real power tracking compensation.

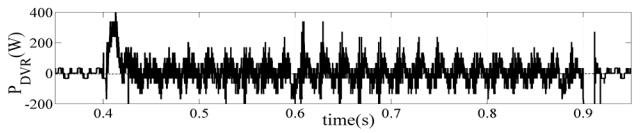


**FIGURE 26.** Real power from the DVR ($P_{DVR}$) during zero-real power tracking compensation.

limit occurred within a period of 280 ms. The DC voltage at any level that was lower than this minimum limit would relatively affect the performance of the compensation. The DVR could not provide a proper compensating voltage anymore, although the precise control actions had been performed in order to correct this situation.

### *B. THE PROPOSED COMPENSATION TEST*

To improve the DVR-based compensation, a different technique, as proposed in this paper, was implemented on the same test rig as described in section A. The same test procedures were carried out in order to compare its performance with the traditional in-phase technique. Satisfactory results, as expected, were seen, as shown in Fig. 24. Direct axis components of both the compensating voltage ($V_{DVRd}$) from the DVR and the load voltage ($V_{Ld}$) remained constant at the desired level for the whole compensation period, from the beginning of the sag period at time t = 0.4 s until the end at time t = 0.9 s. Although the voltage $V_{Ld}$ in this figure was not increased to its pre-sag value, its counterpart quadrature component $V_{Lq}$ was increased correspondingly, as shown in Fig. 25, in order to increase the total magnitude of the load voltage. This was the result of the DVR reaction to quadrature voltage ($V_{DVRq}$), generated as shown in Fig. 25.

Ideally, according to this improved technique – zero real power tracking, none of the real power was injected for the compensation. Practically, however, some small amount of the stored energy was unavoidably supplied to the switching conversion process at the converter. Quite a smaller amount of real power was captured during the compensation, as illustrated in Fig. 26.

Compared with the traditional in-phase technique, the drop in DC-link voltage was slower during the same period, as shown in Fig. 27. A 50 V drop, from 280 V to approximately 230 V, was observed during the period from t = 0.4 s to t = 0.9 s, compared to the 180 V drop shown in Fig. 23 (result of the traditional in-phase technique). At the end of the compensation, this final voltage implies that some energy still remained for further proper compensation at t = 0.9 s if the sag voltage was maintained for longer, meaning the DVR was able to cover a wider range of voltage sags.

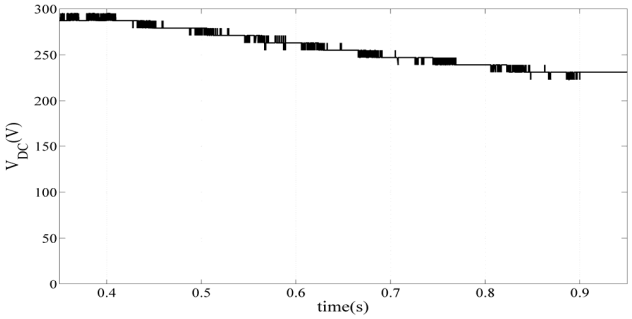


**FIGURE 27.** The DVR DC-side voltage ($V_{DC}$) during zero-real power tracking compensation.

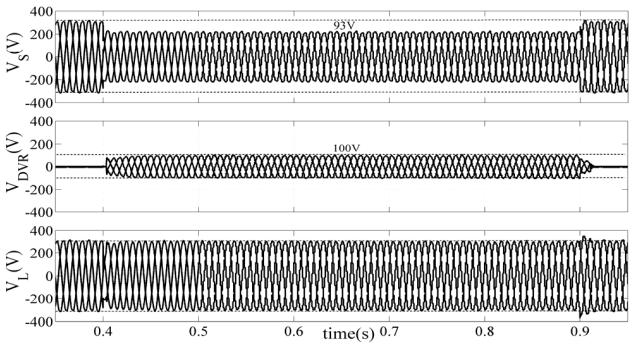


**FIGURE 28.** The overall three-phase voltage signals during zero-active power tracking compensation.

As a result, from the whole compensation process using the proposed zero-real power tracking technique, the end user three-phase load voltage magnitude was therefore maintained in a constant range during the voltage sag disturbance, as illustrated in Fig. 28. Also shown in this figure, with sufficient energy in the DC-link capacitor, the compensating voltage was generated and controlled correctly with more flexibility available for the DVR from the beginning to the end of voltage sag period.

## VI. CONCLUSIONS

It is clear from both the simulation and experimental results illustrated in this paper that the proposed zero-real power tracking technique applied to DVR-based compensation can result in superior performance compared to the traditional in-phase technique. The experimental test results match those proposed using simulation, although some discrepancies due to the imperfect nature of the test circuit components were seen.

With the traditional in-phase technique, the compensation was performed and depended on the real power injected to the system. Then, more of the energy stored in the DC-link capacitor was utilized quickly, reaching its limitation within a shorter period. The compensation was eventually forced to stop before the entire voltage sag period was finished. When the compensation was conducted using the proposed technique, less energy was used for the converter basic switching process.

The clear advantage in terms of the voltage level at the DC-link capacitor indicates that with the proposed technique, more energy remains in the DVR (67% to 14% in the traditional in-phase technique), which guarantees the correct compensating voltage will be provided for longer periods of compensation. With this technique, none (or less) of the real power will be transferred to the system, which provides more for the DVR to cover a wider range of voltage sags, adding more flexible adaptive control to the solution of sag voltage disturbances.

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